Impact of Heat Treatment on a Hetero-Stacked MoS_2/*h*-BN Field-Effect Transistor

Hyunjin Ji, Hojoon Yi, Huong Thi Thanh Nguyen, Sakong Wonkil, Min-Kyu Joo, Hyun Kim, and Seong Chu Lim

***Abstract*— We investigated device properties before and after heat treatment for a hetero-stacked two-dimensional field-effect transistor (FET). In dual-gated monolayer MoS_2 FET using a top h-BN layer and bottom SiO_2 substrate, careful but harsh heat treatment is implemented in high vacuum at 200 °C for 18 h. Under the top-gate bias sweep, the field-effect mobility increases by ∼9 times, and the channel carrier density doubles after the treatment. The heat treatment effect is more noticeable in the top-transferred h-BN than in the bottom SiO_2 layer, because it leads to homogeneous adhesion between the layers by diminishing the adverse effects of interfacial bubbles or adsorbates. A top-gate dielectric capacitance for h-BN of 55 fF is increased to ∼70 fF after the treatment, which is comparable to the theoretical value. This indicates that strong capacitive coupling for the top gate is formed, as confirmed by the capacitance-voltage measurement.**

***Index Terms*— Intensive heat treatment, monolayer MoS_2, dual-gate FET, capacitive coupling, interfacial adsorbates.**

I. Introduction

SINCE the stacking of two-dimensional (2-D) materials for heterostructures became widely known [1]–[4], numerous studies of 2-D materials such as transition metal dechalcogenides (TMDs), graphene, and hexagonal boron nitride (*h*-BN) have been conducted for application. With the advantages of the sizable and reproducible growth of materials, large direct energy band gap, and flexibility, monolayer TMDs such as MoS_2 and WS_2 have been applied in various studies of electronic, magnetic, and optical fields [5]–[10]. However, when stacking several layers, bubbles or adsorbates were inevitably formed at the interface, promoting a variety of subsequent studies [11]–[14].

Existing studies of interfacial bubbles produced by 2-D material transfer have mainly dealt with the issues of heating effect, content, and influence of environmental humidity [15]. Initial studies mostly assumed that the interfacial bubbles were filled with gas, but since Geim *et al*. suggested that the interior was filled with hydrocarbons or water [14], [16], further investigations have supported this assertion [11], [15]. Aside from the importance of analyzing the characteristics of interfacial bubbles, there has been little research on the effect of interfacial bubbles on device characteristics. Interfacial obstacles cause inhomogeneous adhesion between layers, which brings about uneven charge distribution inside the channel of an FET, making it difficult to accurately characterize the device parameters and largely degrading the performance of the device.

Hence, we fabricated chemical vapor deposition (CVD)-grown monolayer MoS_2 dual-gated FET on an Si/SiO_2 substrate with a top-covered *h*-BN layer to investigate the interfacial properties. The quantitative analysis of the influence of interfacial obstacles on the device and its elimination method are provided in this study. As expected, the intensive heat treatment was much more effective in improving the interfacial properties with the transferred *h*-BN at the top rather than with the bottom SiO_2. After the treatment, *h*-BN produced nearly the same capacitance value as the theoretical value, which is improved by more than 30 % than before annealing, and resulted in an increase in the carrier mobility by ∼9 times and a doubling of the channel charge density.

II. Experiment

For the reliability of the TMD FET fabrication, in this study, CVD-grown monolayer MoS_2 is used as a semiconducting channel [17], whose property is verified with a Raman spectrum in Fig. 1(a). The difference in the Raman shift $\sim$18.2 cm^{-1} between the $E^1{}_{2g}$ peak and A_{1g} peak is obtained from monolayer MoS_2 [18], [19]. In processes for the FET fabrication, the source and drain electrodes are made on a transferred monolayer MoS_2 using the conventional electron beam lithography technique (① ②). Then, the 30.7 nm thick mechanically exfoliated multilayer *h*-BN on a different substrate is transferred onto the MoS_2 device using the PMMA carrying-layer method to serve as a top-gate dielectric [20]. *h*-BN is advantageous both for easy tracking of gate capacitance changes, a few tens of fF, and for a low density of charged

Manuscript received July 22, 2019; revised August 5, 2019; accepted August 5, 2019. Date of publication August 26, 2019; date of current version September 25, 2019. This work was supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education under Grant NRF-2019R1A2C1010742. The review of this letter was arranged by Editor E. A. Gutiérrez-D. *(Corresponding authors: Hyunjin Ji; Seong Chu Lim.)*

H. Ji is with the Department of Energy Sciences, Sungkyunkwan University (SKKU), Suwon 16419, South Korea, and also with the Institute of New Paradigm of Energy Science Convergence, SKKU, Suwon 16419, South Korea (e-mail: hjin.ji@skku.edu).

H. Yi, H. T. T. Nguyen, S. Wonkil, H. Kim, and S. C. Lim are with the Department of Energy Science, Sungkyunkwan University (SKKU), Suwon 16419, South Korea, and also with the Center for Integrated Nanostructure Physics, Institute for Basic Science (IBS), Suwon 16419, South Korea (e-mail: seonglim@skku.edu).

M-.K. Joo is with the Department of Applied Physics, Sookmyung Women's University, Seoul 04310, South Korea.

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2019.2936233

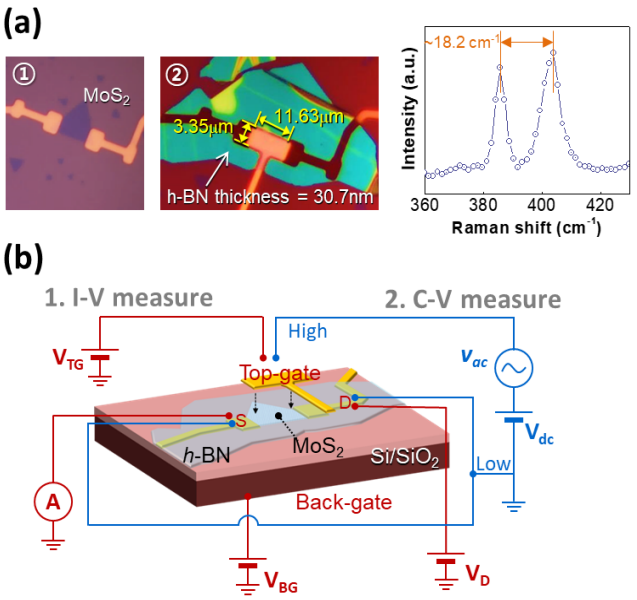

Fig. 1. (a) Photomicrographs of CVD-grown MoS_2 device before top gate creation (①) and the final state of the MoS_2 DG FET (②) with Raman spectrum on MoS_2 (right) and (b) the three-dimensional schematic of the device on Si/SiO_2 and the electrical connection of diagram for measurements.

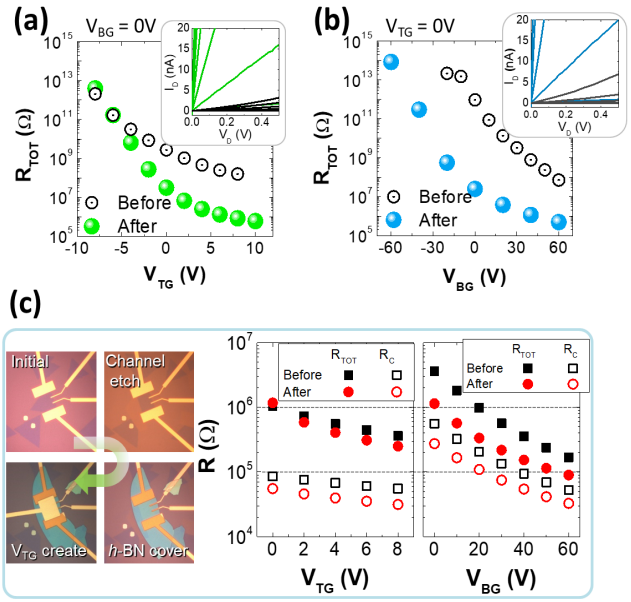

Fig. 2. Comparison of channel conductance corresponding to the inset of I_D-V_D curves before and after heat treatment. (a) R_{TOT} values for V_{TG} and (b) R_{TOT} for V_{BG}. (c) The contact resistance study from a 4-terminal device.

impurities when compared to 300-nm thick SiO_2 layer and high-k dielectric materials [21], [22]. The completed MoS_2 dual-gated (DG) FET is shown in Fig. 1(a), and the channel dimension is marked inside. A three-dimensional schematic of the device in Fig. 1(b) clarifies the device structure, with the electrical connection for the capacitance-voltage and current-voltage measurement diagrams.

III. Results and Discussion

All electrical properties of the device were measured at room temperature, in a high vacuum of $\sim 10^{-7}$ Torr. After the reference measurement, the device was annealed at 200 °C for 18 h in vacuum. First, the device resistance values are compared in the plots of I_D-V_D at different V_{TG} values and different V_{BG} values, in Fig. 2(a) and (b), respectively, before and after thermal annealing. The output curves of I_D-V_D exhibit remarkably improved electrical conductance after annealing, for both V_{TG} and V_{BG}. From the output curves for V_{TG} in the inset of Fig. 2(a), the V_{TG} values were modulated from -8 V to $+8$ V before annealing and from -8 V to $+10$ V after annealing, in 2 V increments, where $V_{BG} = 0$ V. Each graph results in a device total resistance (R_{TOT}) for V_{TG}. The comparison of R_{TOT} shows that the values are reduced by approximately 100 times for V_{TG} after annealing. Meanwhile, the output curves and R_{TOT} values in Fig. 2(b) exhibit the channel property of V_{BG}. Before annealing, V_{BG} changed from -30 V to 60 V in 10 V increments, and it changed from -60 V to $+60$ V in 10 V increments after annealing. During all measurements for V_{BG}, $V_{TG} = 0$ V. Similar to the characteristics for V_{TG}, the R_{TOT} for V_{BG} is considerably reduced after annealing.

To investigate the effect of thermal annealing on a contact resistance (R_C) in detail, we additionally fabricated a 4-terminal test device with channel dimensions similar to that in Fig. 1(a). A reactive ion etching (RIE) process was inevitably required to accurately define channel dimensions in the test device. On the left side of Fig. 2 (c), microscope images of each step are provided. The thermal annealing was implemented for more than 12 h at 200 ° and the resultant R_{TOT} (closed symbols) and contact resistance (R_C, open symbols) are compared for V_{TG} and V_{BG} in right-hand plots of Fig. 2(c). Considering the percentage of R_C with respect to R_{TOT}, the rates of change after annealing were within 10 % for V_{TG} and V_{BG}. Considering that the channel property itself was considerably enhanced, it is true that the heat treatment improves the contact property to some extent, although there appears to be other factors contributing significantly to the improvement in performance.

The effect of heat treatment for the dual-gated monolayer MoS_2 FET is mainly investigated in the transfer curves and capacitance-voltage (C-V) properties in this experiment, with the swept V_{TG} under the fixed V_{BG}. From the transfer curves, I_D-V_{TG}, V_{BG} increases from -30 V to $+60$ V in 10 V increments before annealing (orange color), and V_{BG} increases from -60 V to $+60$ V in 10 V increments after annealing (yellow-green color). The electrical conductance is significantly improved after annealing in Fig. 3(a). Specifically, at $V_{TG} - V_{TH} (= V_{GT}) = 10$ V and $V_{BG} = 40$ V, the value of I_D rises approximately four times, from 0.53 μA to 2.19 μA, after annealing. Moreover, when $V_{GT} = 10$ V and $V_{BG} = 60$ V, I_D increases 2.7 times from 0.83 μA to 2.21 μA. This signifies that although the structure and measurement environment of the device have not changed at all, after annealing, the same vertical gate voltages induce more carriers inside the channel.

From the transfer curves, the earlier turn-on of the device after annealing is observed as well, and it is characterized by V_{TH}. We extracted V_{TH} using the capacitance derivative

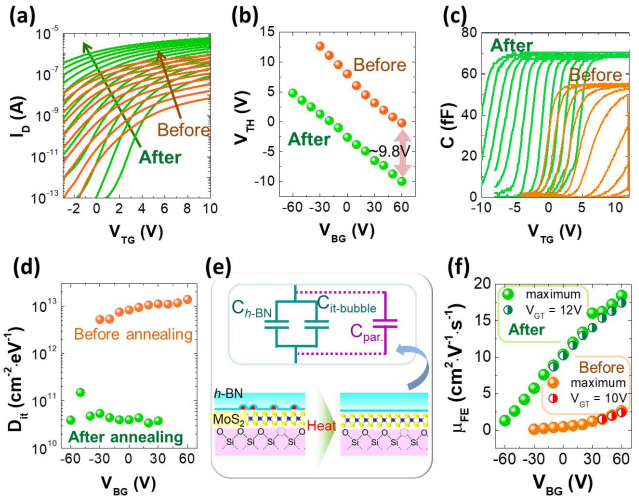

Fig. 3. Device characteristics before (orange) and after (yellow-green) annealing under V_{TG} sweep with the fixed V_{BG} and at V_D = 0.5. (a) Transfer curves, (b) threshold voltages (V_{TH}), (c) top-gate capacitance, (d) the interface trap density (D_{it}), (e) the equivalent capacitance model in this device, and (f) μ_{FE}.

method ($dC_g \cdot dV_{TG}^{-1}$) in Fig. 3(b). From the previous study of SOI MOSFETs for V_{TH} analysis, the capacitance derivative method is well-known to be the most reliable and the most physically accurate among the representative V_{TH} extraction methods, because it originates from the unified charge-control model [23], [24]. The evident negative shift of V_{TH} after annealing is an average of approximately 10 V, and the rate of change for V_{BG}, namely the slope of V_{TH} versus V_{BG}, is similar before and after annealing.

Previously, the effects of thermal annealing in nanomaterial FETs have been mostly studied in terms of the improvement in the contact resistance [25]–[28]. However, when stacking 2-D materials in multiple layers, it is important to control the interface characteristics between the layers, which is the major factor in device performance [12], [29], [30]. This is because interfacial bubbles or residues, as well as weak van der Waals force interactions between materials, exist. In the following discussion, we focus on the C-V measurement and analysis, showing the interface characteristics in the device.

Because the back-gate dielectric capacitance of a 300-nm thick SiO_2 layer is too small to accurately investigate the change pattern, all capacitance studies were performed on a 30-nm thick h-BN under V_{TG} sweep. The thermal annealing improves the C-V properties, as represented in Fig. 3(c). As described in the V_{TH} characteristics for the earlier device turn-on, the shifts in the C-V curves are quite apparent as well. The previous value of ~55 fF in saturation increases to ~70 fF after annealing. Considering that the calculated capacitance value of top h-BN with a dielectric constant of 3~4 [22], [31]–[33] is 65~87 fF, the heat treatment seems to very effectively remove the deterioration factor.

We also calculated the interface trap density D_{it} for h-BN from the subthreshold slope for V_{TG} [34], where we used the measured C_g values, instead of the calculated one. While the D_{it} before annealing ranges around 10^{13} cm^{-2}·eV^{-1}, it considerably reduces to approximately 4×10^{10} cm^{-2}·eV^{-1} after annealing, as plotted in Fig. 3(d). Previous studies of TMD FETs on D_{it} show that the value of ~10^{10} cm^{-2}·eV^{-1} in this study highlights the interface properties for the top gate h-BN layer, rather than SiO_2 [34].

A simple equivalent capacitance model for the V_{TG} sweep is illustrated at the top of Fig. 3(e), and a device cross-section is drawn at the bottom. In the model, C_{h-BN}, C_{it-BA}, and $C_{par.}$ are the effective capacitance values for the h-BN layer, the capacitance by bubbles or adsorbates, and the parasitic capacitance by the back-gate field, respectively. $C_{par.}$ is computed from the difference in the saturation value according to the V_{BG}, which is negligibly small, as shown in Fig. 3(c). The bubbles or adsorbates between h-BN and MoS_2 reduce the effective area for capacitive coupling of channel to V_{TG}. Therefore, the channel charges induced by the top-gate field are reduced, and the device performance degrades. The channel carrier density (N_{acc}) calculated from the C-V plots supports this fact. The maximum value of V_{GT} measured at V_{BG} = 0 V before annealing was 4 V and the N_{acc} value at the same condition was increased 2.57 times from 9.2×10^{11} cm^{-2} to 2.4×10^{12} cm^{-2} after annealing. Generally, the electrical conductivity is proportional to the mobility and carrier density of the material. Therefore, both can explain the considerably increased conductivity after annealing.

In the FET operation principle, the field effect mobility μ_{FE} of the device can be calculated using the measured capacitance values, as shown in Fig. 3(f). We exhibited the comparison results at the maximum value and at V_{GT} = 10 V in the figure. When V_{GT} = 10 V, the μ_{FE} increased 9.6 times and 7.7 times for V_{BG} = 40 V and 50 V, respectively. Comparing the maximum values based on V_{GT}, it increased 7.2 times from 2.4 cm^2·V^{-1}·s^{-1} to 17.4 cm^2·V^{-1}·s^{-1} at V_{BG} = 60 V and V_{GT} = 10 V as shown in Fig. 3(f).

The results above signify that when V_{BG} is low before annealing, V_{TG} rarely generates an effective channel because of the poor interface between h-BN and MoS_2. However, after the improvement of the top interface characteristics by heat treatment, the top-gate field controls the channel actively even in the very low V_{BG} region.

IV. Conclusion

For reliable device operation using 2-D TMD materials, several strategies, such as multi-layer stacking and the use of surface-inert h-BN as a gate dielectric, have been studied to date. However, implementing actual performance improvement is as important as suggesting a new method. Through the persistent annealing for more than 10 hours in a monolayer MoS_2 DG FET, we have demonstrated that the capacitive coupling between the h-BN and MoS_2 channels is significantly improved owing to the reduction of probable parasitic capacitive substances, as evidenced by the C-V characteristics. The ultimate performance of h-BN was almost realized, exhibiting a capacitance value similar to the calculated value after the annealing. Finally, the top-gate field through h-BN in an FET induced a channel charge that was doubled and produced a field effect mobility that was approximately nine times greater. This study shows the effect of interfaces on the performance of low-dimensional miniaturized devices, and this will serve as a valuable example for a follow-up TMD study.

REFERENCES

[1] A. K. Geim and I. V. Grigorieva, "Van der Waals heterostructures," *Nature*, vol. 499, no. 7459, pp. 419–425, Jul. 2013.

[2] K. S. Novoselov, A. Mishchenko, A. Carvalho, and A. C. Neto, "2D materials and van der Waals heterostructures," *Science*, vol. 353, no. 6298, Jul. 2016, Art. no. aae9439.

[3] C. H. Lee, "Atomically thin p–n junctions with van der Waals heterointerfaces," *Nature Nanotechnol.*, vol. 9, no. 9, pp. 676–681, Aug. 2014.

[4] Y. Liu, N. O. Weiss, X. Duan, H.-C. Cheng, Y. Huang, and X. Duan, "Van der Waals heterostructures and devices," *Nature Rev. Mater.*, vol. 1, no. 9, Sep. 2016, Art. no. 16042.

[5] F. Withers, O. Del Pozo-Zamudio, A. Mishchenko, A. P. Rooney, A. Gholinia, K. Watanabe, T. Taniguchi, S. J. Haigh, A. K. Geim, A. I. Tartakovskii, and K. S. Novoselov, "Light-emitting diodes by band-structure engineering in van der Waals heterostructures," *Nature Mater.*, vol. 14, no. 3, pp. 301–306, Feb. 2015.

[6] X. Zhou, X. Hu, J. Yu, S. Liu, Z. Shu, Q. Zhang, H. Li, Y. Ma, H. Xu, and T. Zhai, "2D layered material-based van der Waals heterostructures for optoelectronics," *Adv. Funct. Mater.*, vol. 28, no. 14, Apr. 2018, Art. no. 1706587.

[7] Z. X. Guo, Y. Chen, H. Zhang, J. Wang, W. Hu, S. Ding, D. We. Zhang, P. Zhou, and W. Bao, "Independent band modulation in 2D van der Waals heterostructures via a novel device architecture," *Adv. Sci.*, vol. 5, no. 9, Sep. 2018, Art. no. 1800237.

[8] R. Q. Cheng, F. Wang, L. Yin, Z. Wang, Y. Wen, T. A. Shifa, and J. He, "High-performance, multifunctional devices based on asymmetric van der Waals heterostructures," *Nature Electron.*, vol. 1, no. 6, pp. 356–361, Jun. 2018.

[9] C. Li, P. Zhou, and D. W. Zhang, "Devices and applications of van der Waals heterostructures," *J. Semicond.*, vol. 38, no. 3, Mar. 2017, Art. no. 031005.

[10] X. Wang, W. M. Lü, A. Annadi, Z. Q. Liu, K. Gopinadhan, S. Dhar, T. Venkatesan, and A. Annadi, "Magnetoresistance of two-dimensional and three-dimensional electron gas in $LaAlO_3$/$SrTiO_3$ heterostructures: Influence of magnetic ordering, interface scattering, and dimensionality," *Phys. Rev. B, Condens. Matter*, vol. 84, no. 7, Aug. 2011, Art. no. 075312.

[11] D. A. Sanchez, Z. Dai, P. Wang, A. Cantu-Chavez, C. J. Brennan, R. Huang, and N. Lu, "Mechanics of spontaneously formed nanoblisters trapped by transferred 2D crystals," *Proc. Natl. Acad. Sci. USA*, vol. 115, no. 31, pp. 7884–7889, Jul. 2018.

[12] T. Uwanno, Y. Hattori, T. Taniguchi, K. Watanabe, and K. Nagashio, "Fully dry PMMA transfer of graphene on h-BN using a heating/cooling system," *2D Mater.*, vol. 2, no. 4, Dec. 2015, Art. no. 041002.

[13] E. M. Alexeev, A. Catanzarom, O. V. Skrypka, P. K. Nayak, S. Ahn, S. Pak, J. Lee, J. I. Sohn, O. S. Novoselov, H. S. Shin, and A. I. Tartakovskii, "Imaging of interlayer coupling in van der Waals heterostructures using a bright-field optical microscope," *Nano Lett.*, vol. 17, no. 9, pp. 5342–5349, Sep. 2017.

[14] S. J. Haigh, A. Gholinia, R. Jalil, S. Romani, L. Britnell, D. C. Elias, K. S. Novoselov, L. A. Ponomarenko, A. K. Geim, and R. Gorbachev, "Cross-sectional imaging of individual layers and buried interfaces of graphene-based heterostructures and superlattices," *Nature Mater.*, vol. 11, no. 9, pp. 764–767, Jul. 2012.

[15] F. Pizzocchero, L. Gammelgaard, B. S. Jessen, J. M. Caridad, L. Wang, J. Hone, P. Bøggild, and T. J. Booth, "The hot pick-up technique for batch assembly of van der Waals heterostructures," *Nature Commun.*, vol. 7, Jun. 2016, Art. no. 11894.

[16] E. Khestanova, F. Guinea, L. Fumagalli, A. K. Geim, and I. V. Grigorieva, "Universal shape and pressure inside bubbles appearing in van der Waals heterostructures," *Nature Commun.*, vol. 7, Aug. 2016, Art. no. 12587.

[17] Y. Lee, S. Park, H. Kim, G. H. Han, Y. H. Lee, and J. Kim, "Characterization of the structural defects in CVD-grown monolayered MoS_2 using near-field photoluminescence imaging," *Nanoscale*, vol. 7, no. 28, pp. 11909–11914, Jun. 2015.

[18] H. Li, Q. Zhang, C. C. R. Yap, B. K. Tay, T. H. T. Edwin, A. Olivier, and D. Baillargeat, "From bulk to monolayer MoS_2: Evolution of Raman scattering," *Adv. Funct. Mater.*, vol. 22, no. 7, pp. 1385–1390, Apr. 2012.

[19] Y.-H. Lee, X.-Q. Zhang, W. Zhang, M.-T. Chang, C.-T. Lin, K.-D. Chang, Y.-C. Yu, J. T.-W. Wang, C.-S. Chang, and L.-J. Li, "Synthesis of large-area MoS_2 atomic layers with chemical vapor deposition," *Adv. Mater.*, vol. 24, no. 17, pp. 2320–2325, May 2012.

[20] R. Frisenda, E. Navarro-Moratalla, P. Gant, D. P. De Lara, P. Jarillo-Herrero, R. V. Gorbachev, and A. Castellanos-Gomez, "Recent progress in the assembly of nanodevices and van der Waals heterostructures by deterministic placement of 2D materials," *Chem. Soc. Rev.*, vol. 47, no. 1, pp. 53–68, Jan. 2018.

[21] Q. A. Vu, S. Fan, S. H. Lee, M.-K. Joo, W. J. Yu, and Y. H. Lee, "Near-zero hysteresis and near-ideal subthreshold swing in h-BN encapsulated single-layer MoS_2 field-effect transistors," *2D Mater.*, vol. 5, no. 3, Jul. 2018, Art. no. 031001.

[22] J. Wang, F. Ma, and M. Sun, "Graphene, hexagonal boron nitride, and their heterostructures: Properties and applications," *RSC Adv.*, vol. 7, no. 27, pp. 16801–16822, Mar. 2017.

[23] C.-K. Park, C.-Y. Lee, K. Lee, B.-J. Moon, Y. H. Byun, and M. Shur, "A unified current-voltage model for long-channel nMOSFETs," *IEEE Trans. Electron Devices*, vol. 38, no. 2, pp. 399–406, Feb. 1991.

[24] D. Flandre, V. Kilchytska, and T. Rudenko, "$g(m)/I - d$ method for threshold voltage extraction applicable in advanced MOSFETs with nonlinear behavior above threshold," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 930–932, Sep. 2010.

[25] Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, "High performance silicon nanowire field effect transistors," *Nano Lett.*, vol. 3, no. 2, pp. 149–152, Feb. 2003.

[26] K. Byon, D. Tham, J. E. Fischer, and A. T. Johnson, "Systematic study of contact annealing: Ambipolar silicon nanowire transistor with improved performance," *Appl. Phys. Lett.*, vol. 90, no. 14, Apr. 2007, Art. no. 143513.

[27] O. Balci and C. Kocabas, "Rapid thermal annealing of graphene-metal contact," *Appl. Phys. Lett.*, vol. 101, no. 24, Dec. 2012, Art. no. 243105.

[28] F. L. Wang, P. Stepanov, M. Gray, and C. N. Lau, "Annealing and transport studies of suspended molybdenum disulfide devices," *Nanotechnology*, vol. 26, no. 10, Mar. 2015, Art. no. 105709.

[29] H. Lim, S. I. Yoon, G. Kim, A. R. Jang, and H. S. Shin, "Stacking of two-dimensional materials in lateral and vertical directions," *Chem. Mater.*, vol. 26, no. 17, pp. 4891–4903, Aug. 2014.

[30] D. G. Purdie, N. M. Pugno, T. Taniguchi, K. Watanabe, A. C. Ferrari, and A. Lombardo, "Cleaning interfaces in layered materials heterostructures," *Nature Commun.*, vol. 9, Dec. 2018, Art. no. 5387.

[31] K. K. Kim, A. Hsu, X. Jia, S. M. Kim, Y. Shi, M. Dresselhaus, T. Palacios, and J. Kong, "Synthesis and characterization of hexagonal boron nitride film as a dielectric layer for graphene devices," *ACS Nano*, vol. 6, no. 10, pp. 8583–8590, Sep. 2012.

[32] A. F. Young, C. R. Dean, I. Meric, S. Sorgenfrei, H. Ren, K. Watanabe, T. Taniguchi, J. Hone, K. L. Shepard, and P. Kim, "Electronic compressibility of layer-polarized bilayer graphene," *Phys. Rev. B, Condens. Matter*, vol. 85, no. 23, Jun. 2012, Art. no. 235458.

[33] A. Laturia, M. L. Van de Put, and W. G. Vandenberghe, "Dielectric properties of hexagonal boron nitride and transition metal dichalcogenides: From monolayer to bulk," *2D Mater. Appl.*, vol. 2, Mar. 2018, Art. no. 6.

[34] M. K. Joo, B. H. Moon, H. Ji, G. H. Han, H. Kim, G. Lee, S. C. Lim, Y. H. Lee, and D. Suh, "Electron excess doping and effective Schottky barrier reduction on the MoS_2/h-BN hetero-structure," *Nano Lett.*, vol. 16, no. 10, pp. 6383–6389, Sep. 2016.