Annihilation Behavior of Planar Defects on Phosphorus-Doped Silicon at Low Temperatures

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The planar defect behavior and phosphorus (P) diffusion of P-doped silicon (Si) thin film on monocrystalline Si with annealing was investigated by high-resolution transmission electron microscopy. These images indicate that the as-deposited Si thin film crystallizes with many planar defects, such as stacking faults and twin boundaries. Secondary ion mass spectroscopy and atom probe tomography reveal that P atoms are segregated to the planar defects and diffuse out the Si substrate at 600 °C. The solubility of P atoms has an influence on the rearrangement of Si atoms, which leads to the annihilation of the defects in the deposited Si thin film.

Keywords: Phosphorus Diffusion, Stacking Fault, Interface, Doped Silicon.

1. INTRODUCTION

Semiconductor devices have been developing with reduced design rules, increased density, and improved performance. Device size is at the limit of lithography techniques ~20 nm technology. In such nanosized devices, the interfaces and crystalline defects are strongly in need of control.

The manufacturing process for fabricating phosphorus (P)-doped polysilicon and silicon (Si) selective epitaxial growth plugs continues to receive more attention as a key factor for high-performance semiconductor devices.¹⁻⁹ A variety of physical phenomena, such as P diffusion by subsequent heat treatment, interfacial defect segregation, and the creation and destruction of crystal defects, is expected to occur within a poly-Si plug structure. Therefore, high-quality poly-Si contacts are formed that should be observed closely to increase the understanding of these phenomena. In particular, the interface control technology of this small area is crucial to obtain the desired electrical properties. The defective surfaces cause considerable planar defects during the epitaxial Si growth process. The occurrence of planar defects in the epilayer may impair the device properties by reducing the lifetime of generated charge carriers and increasing leakage currents.¹⁰

In reality, however, contact Si thin film contains various planar defects because the surface defects, which are caused by misaligned structures for high device density and etch patterning damage, remain, even though subjected to a high-performance surface cleaning process. Therefore, we investigated the behavior of planar defects of P-doped Si on damaged Si substrates through annealing.

2. EXPERIMENTAL DETAILS

We used 12 inch, p-type Si wafers with a 0.5–20 Ω·cm resistivity. Wet and dry etch damage was introduced to the Si substrate before proceeding with dry cleaning, to create an environment like the interface area of the contact structure in a semiconductor. Then the wet chemical oxide formed on the damaged Si surface. Next, the prepared sample was dry-cleaned. P-doped Si thin film was deposited onto the sample wafers using a low-pressure chemical vapor deposition system at 500 °C.

The P-doped Si thin films were annealed using a tube furnace at temperatures between 200 and 600 °C for 30 min in a N₂ atmosphere of 1 torr at the rate of...
100 °C/min. To obtain the elemental distribution in the P-doped Si thin films, depth profiles were taken via secondary ion mass spectroscopy (SIMS, IMS 7f magnetic sector, Cameca). The SIMS characterizations were performed with a Cs+ ion beam energy of 6 kV and a current of 20 nA.

Three dimensional (3D) elemental distributions were obtained using atom probe tomography (APT, LaWaTAP, Cameca). The APT characterizations were performed with a laser wavelength of 343 nm, pulse repetition rate of 100 kHz, and specimen temperature of 30 K. The samples for APT measurement were prepared using a dual-beam focused ion beam (FIB, Helios, FEI) with a tip diameter of 40 nm.

Bright field and high-resolution transmission electron microscopy (HRTEM) images were obtained using JEOL’s JEM-2100F at an accelerating voltage of 200 kV. The thermal behavior of the thin films was investigated while increasing the temperature from 25 °C to 750 °C using a JEOL EM-31050 double-tilt heating holder and JEM-3011 at an accelerating voltage of 300 kV. The samples for the cross-sectional TEM measurements were mechanically polished to a thickness of approximately 10 μm, and then mounted on a molybdenum TEM grid followed by ions milled at 3.5 kV using Ar+ ions (Precision Ion Polishing System II, Gatan).

3. RESULTS AND DISCUSSION

3.1. Results

Figure 1 shows cross-sectional TEM images of P-doped Si thin film after dry cleaning at various annealing temperatures. Figure 1(a) shows considerable planar defects in the film. Some SFs were propagated into the film from damaged sites on the substrate surface. Most SFs observed on the (111) planes were generated at the substrate surface.11 The morphology of the P-doped Si/Si substrate interface has a roughly wave-shaped grooved surface morphology resulting from the pre-cleaning etch processes. Up through an annealing temperature of 400 °C, the planar defects of the deposited film remained the same. However, at an annealing temperature of 600 °C, the HRTEM image of the thin film shows a dramatic change—the elimination of planar defects.

Figures 2(b–d) show the SIMS results for P diffusion in poly-Si thinfilm/Si substrate by N2 annealing for temperatures of 200, 400 and 600 °C, respectively. The peak intensity of P in Si is approximately 500 k counts, and the oxygen (O) and fluorine (F) peaks into the interface are caused by residual elements left after dry cleaning, as shown in Figure 2(a).

Although the P concentration distribution appears not to change until 400 °C, Figure 2(d) shows that both surface P and interface P concentrations in the deposited Si thin film are higher than the P concentration in the bulk Si thin film, resulting in a P peak. This signifies the segregation of the P in the interface layer and surface native oxide from the deposited Si thin film after annealing at 600 °C. Additionally, the P concentration in the Si substrate was increased by more than 2.5 orders of magnitude at a depth of about 60 nm. Annealing at 600 °C primarily led to dramatic changes in the P distribution into both the deposited Si thin film and the Si substrate.

Figure 3(b) shows an HRTEM image of a Si thin film annealed at 400 °C. The magnified HRTEM image in Figure 3(b) marked of the rectangle area in Figure 3(a), indicates that the Si thin film has SFs and twin boundaries as shown in Figure 3(b). The normal stacking sequence is ABCABC in the face centered cubic structures, but the SF reveals that one of the A planes is missing, which introduces an irregularity such as ABCBC. Twin boundaries shows that the planes participating in such defects form at 70.5° with respect to the {111} mirror plane, and that the sequence becomes BCACB or CBABC.

Figure 3(d) shows an HRTEM image of a film annealed at 600 °C. Regions A and B in Figure 3(d) are a Si substrate and a deposited P-doped Si thin film, respectively. The crystal structure of region A is a diamond with a cell dimension of 0.543 nm. This was confirmed by the HRTEM and fast Fourier transform (FFT) images taken in the direction of the [011] zone axis, as shown in Figures 3(e and f). The corresponding HRTEM and FFT images for region B indicate that the region has a crystalline Si phase without planar defects, as shown in Figures 3(g and h).

The APT analysis was used to precisely observe the dopant segregation into planar defects. The segregation

\[ \text{Figure 1. Cross-sectional TEM images of P-doped Si thin film at various annealing temperatures: (a) as deposited, (b) 200 °C, (c) 400 °C, and (d) 600 °C.} \]
of the dopants at grain boundaries in a poly-Si gate was clearly observed with atomic resolution using APT.\textsuperscript{12} Figures 3(c and i) show an enlarged view of the 3-D elemental map around the P-doped Si thin film/Si substrate interface. In these figures, Si atoms are not shown, and the green circles indicate carbon (C) atoms, which are mainly located on the interface and the surface. Figure 3(c) shows that P atoms congregate at the planar defects in the thin film, while most P atoms seem to diffuse out to segregate at the interface, as well as to move to the Si substrate, after annealing at 600 °C as shown in Figure 3(i).

Figure 4 shows in-situ HRTEM images of a Si thin film obtained with increasing temperatures, from room temperature to 750 °C. The HRTEM images were acquired from the same area as shown in Figures 4(a–e). The pristine state of the Si thin film was crystalline state, with planar defects. The regions indicated by the yellow arrows have evidence a crystalline phase with planar defects from room temperature to 700 °C, but the defects in that region start to vanish at 750 °C.

3.2. Discussion

In small contact of device, the dry cleaning method is preferred to create a hydrophobic H-terminated surface, which prevents oxidation and readily controls the selectivity of the etch rate. Dry cleaning is also suitable for allowing subsequent Si deposition processes to proceed in a short time, without additional processes such as rinsing, blowing, and drying. Therefore, the surface was cleaned by dry cleaning here.

From the TEM image in Figure 1(a), the interface has a highly curved morphology and a discontinuous interfacial layer, which is composed of residual O and F, as shown in Figure 2(a), although the dry cleaning process can remove an oxide layer of 50 Å. This phenomenon can be explained by the residual F elements on the substrate surface, which are a by-product of the dry cleaning process, and lead to accelerated native oxide re-growth.

Therefore, it is reasonably estimated that the defective state and residual oxide of the interface cause too great a density of planar defects in the deposited P-doped Si thin film in our experiment, since most crystal defects in the thin film were directly caused by defects or contamination at the substrate surface and the interface, even though eventually removed by chemical oxidation.\textsuperscript{11}

From the point of view of P distribution, it is well known that grain boundaries are also low energy sites, at which P atoms can be preferentially located as dopants, in the case of poly-Si. P dopants into the epitaxial Si thin film with SFs can be similarly explained. It has been theoretically expected that P segregation will be observed at the SFs. Justo et al. computed the vacancy formation energy at both crystalline-like (CL) and SF sites. The vacancy formation energy of CLs is 3.06 eV, while the value for SFs is smaller by 0.23 eV. They also calculated the segregation energy, which is the difference of the total calculated energy for impurities in the CL and the SF; for P, this energy is 0.09 eV. These results show that the

Figure 2. SIMS results for P diffusion in P-doped Si thin film/Si substrates by N\textsubscript{2} annealing for temperatures of (a) as-deposited, (b) 200 °C, (c) 400 °C and (d) 600 °C, using a ramp rate of 100 °C/min and a hold time of 30 min.
formation energies of intrinsic defects and impurities are lower at SFs, compared with CLs. Therefore, SFs should have a larger concentration of defects. In addition, n-type dopant segregation on SFs are explained as a reduction in the SF energy, which results from decreasing the layer displacement around the SF, by dopant agglomeration on the SF, and from reducing high electronic energy on the SF, by attractive electronic interactions of n-type dopants with the SF. Therefore, it is reasonable to expect that, during deposition on the Si substrate, most P atoms will segregate around planar defects in the P-doped Si thin film. To summarize so far, it is estimated that P-doped Si thin film has a few planar defects, caused by residual oxidation and damage on the interface, and that P segregates on those planar defects. From the annealing test, it is observed that the P diffusion occurred simultaneously with the planar defects in the P-doped Si thin film annealed at 600 °C. This phenomenon is explained below.

The elimination of SFs as planar defects has been previously observed by several researchers. The apex of the tetrahedron structure on the interface collapses to the correct stacking, so the elimination proceeds toward the surface. The elimination begins locally from the layer surface and proceeds to the apex of the tetrahedron structure in the {111}-oriented layer case. On the other hand, the elimination occurs locally, not only from the layer surface, but also from partial dislocation of the SF under the surface of the growth layer in a {100}-oriented Si epitaxial layer, because of the high temperature annealing process above 800 °C.

Annihilation of SFs at relatively low temperatures (~600 °C) in this experiment can be explained by a heavy P-doping effect. The annihilation mechanism of SFs by P-doping is strongly associated with the vacancy concentration in Si. The vacancy concentration is influenced by factors such as treatment temperature, donor doping, and stress by solute lattice contraction of an impurity in the Si. Of these factors, we focused on donor doping. When P atoms were diffused into Si having SFs, and the P concentration exceeded the intrinsic carrier concentration, the SFs in the diffused layers were annihilated for a short time due to vacancy generation and Si self diffusion. In other words, the annihilation was enhanced by the donor-induced vacancies.

P-doped Si for interconnect has excessive P dopants due to low resistance. Since the P solubility limit concentration...
determined according to the temperature, excessive P is likely to be segregated in the low energy region. However, the solubility limit of P in Si increases proportionately to temperature. The solubility of P in Si increases at 600 °C, particularly when the deposition temperature is 500 °C, at which time the increased P is diffused into the Si thin film. After all, injected P atoms lead to increased vacancy concentration, which reduces the SF.

4. CONCLUSION
In this study, the relationship between changes in behavior of planar defects and P diffusion in highly P-doped Si for interconnecting Si plugs as a function of annealing was investigated. Damage was inflicted on the Si substrate to simulate the production environment, and then P-doped Si was deposited after dry cleaning. It was confirmed that the planar defects were created by the impact of the damage treatment. At the same time, the diffusion behavior of the P atoms in the Si thin film did not diffuse through the vacancies. Shortly after the planar defects were created by heat treatment was observed by the in-situ TEM, and began at about 750 °C.

From the experimental results, it was found that P atoms segregated to the lower energy region (planar defects) from the Si thin film, and the concentration of P atoms in Si thin film increased proportionally with temperature. Vacancy generation in Si thin films was promoted by a P solubility increase, and the planar defects were eliminated by Si self-diffusion through the vacancies. Shortly after the planar defects disappeared, the P also diffused out substrate Si.

The deeper understanding of this behavior through our study is a major contribution to the development of P-doped Si plugs for the next generation of semiconductor devices.

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References and Notes

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