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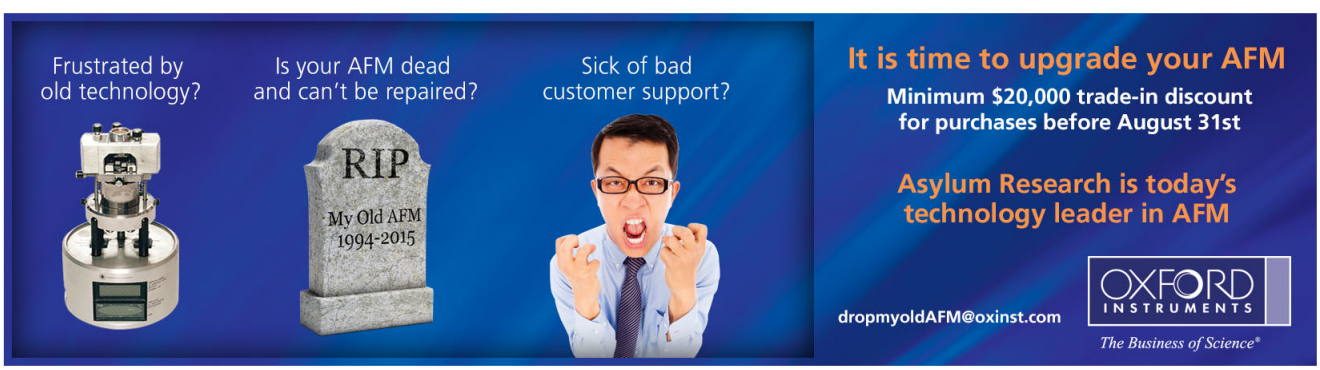

The role of contact resistance in GeTe and $Ge_2Sb_2Te_5$ nanowire phase change memory reset switching current

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Nanowire (NW) structures offer a model system for investigating material and scaling properties of phase change random access memory (PCRAM) at the nanometer scale. Here, we investigate the relationship between nanowire device contact resistance and reset current (I_{reset}) for varying diameters of NWs. Because the reset switching current directly affects possible device density of PCRAM NWs, it is considered one of the most important parameters for PCRAM. We found that the reset switching current, I_{reset}, was inversely proportional to the contact resistance of PCRAM NW devices decreasing as NW diameter was reduced from 250 nm to 20 nm. Our observations suggest that the reduction of power consumption of PCRAM in the sub-lithographic regime can be achieved by lowering the contact resistance. © *2015 AIP Publishing LLC*.
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Phase change random access memory (PCRAM) utilizes thermally induced reversible phase transitions, usually from amorphous to crystalline, in chalcogenide materials. PCRAM has been proposed as a promising candidate for next generation nonvolatile memory technology as an alternative to flash memory and dynamic random access memory.[1,2] Although PCRAM has several advantages such as fast write/read speed, non-volatility, and high endurance, the adoption of PCRAM devices is still hindered by the large reset current required for memory switching. Current limits the scaling of PCRAM, since it must be supplied by a memory cell selector (usually in the form of a transistor or diode) of sufficient area in order to provide the required current.[2] Thus, reducing the programming current is necessary for achieving high-density and low power consumption PCRAM.

In order to decrease the reset current (I_{reset}), cell size scaling is an effective method, since the reduction of active phase change material (PCM) volume is directly related to power consumption used during phase transition.[3–5] Recently there have been several reports on scaling of PCRAM devices based on nanowires (NWs).[6–8]

Nanowire-based PCRAM device can serve as a model system for studying scaling of PCRAM device due to their sub-lithographic size, defect-free single-crystalline structure, and unique geometry.[9,10] Furthermore, one-dimensional NWs are similar to the confined bar-type cell geometry adapted in industrially developed PCRAM.[1] In this study, we investigate the scaling behaviors on the PCRAM by employing horizontal PCRAM test devices that incorporate individual NWs of PCMs including GeTe and $Ge_2Sb_2Te_5$. We discover that the contact resistance between PCMs and metal electrodes is responsible for reduction of I_{reset} in NW PCRAM devices.

Single-crystalline GeTe and $Ge_2Sb_2Te_5$ NWs were synthesized using Au catalyst-mediated gas phase vapor-liquid-solid (VLS) growth. The Au catalyst was prepared by either evaporating a 1 nm thick Au film for thick NWs (50 nm–250 nm diameter) or coating with Au colloids with a diameters of 20–50 nm for thin NWs (28 nm–60 nm diameter). Bulk GeTe and Sb_2Te_3 powders were used as precursors for NW growth. The Au-coated SiO_2/Si substrates were placed downstream in a 1.4-in. diameter horizontal tube furnace with source material, placed in the hot center region. The mixture of argon and nitrogen gas acted as a carrier gas to transport the vapor precursor to the colder furnace region with the gold coated substrate. Before each growth, the quartz tube was evacuated to $<$100 mTorr and flushed with the high-purity nitrogen (N_2) carrier gas repeatedly to limit oxygen contamination. The source material in the form of 50 mg of GeTe power (99.99%, Alfa) for GeTe nanowires and a mixture of 25 mg GeTe powder and 50 mg Sb_2Te_3 powder (99.99%, Alfa) for $Ge_2Sb_2Te_5$ nanowire growth were placed in a boat near the heated center of the furnace. The center of the furnace was heated to 550 °C for 30 min while flowing 50 sccm of Ar and 100 sccm of N_2 as a carrier gases simultaneously. GeTe and $Ge_2Sb_2Te_5$ NWs resulted after 2–4 h of growth time while maintaining a pressure of 100 Torr.

Figures 1(a) and 1(b) show representative scanning electron microscopy (SEM) and transmission electron microscopy (TEM) micrographs of individual $Ge_2Sb_2Te_5$ NWs, respectively. The presence of Au catalyst at the tip of the nanowires, as in the inset of Figure 1(a), suggests that the growth is governed by the VLS mechanism. The crystal structure of grown NWs was also confirmed by x-ray diffraction analysis, not shown here, to be GeTe rhombohedral

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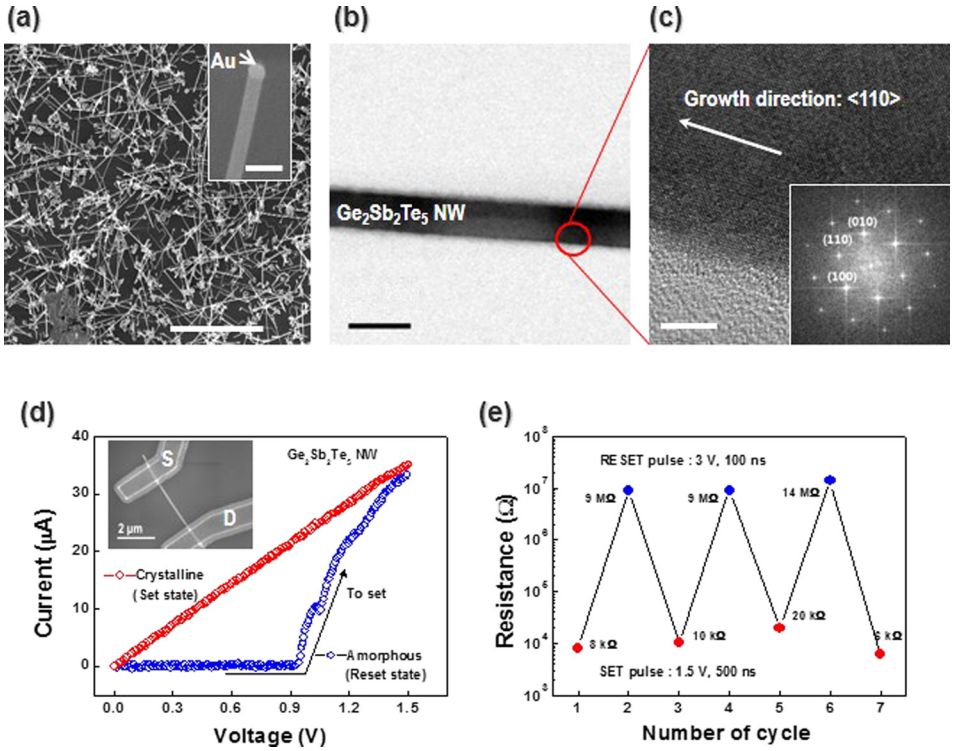

FIG. 1. (a) SEM image after VLS growth of $Ge_2Sb_2Te_5$ nanowires; the scale bar is 10 nm. Inset shows Au cap indicating VLS growth mechanism for nanowires. Inset scale bar is 100 nm. (b) TEM image of 28 nm diameter $Ge_2Sb_2Te_5$ nanowire; the scale bar is 50 nm (c) Magnified TEM of nanowire interface showing (110) direction; scale bar is 5 nm. The inset FFT confirms (110) growth direction. (d) The DC *I-V* characteristics of the $Ge_2Sb_2Te_5$ 28 nm NW. Inset shows fabricated device with source/drain (Ni/Au) Ohmic contacts. (e) Repeated resistance measurements of $Ge_2Sb_2Te_5$ 75 nm NW phase change memory device. Device was switched between high- and low-resistive states using respective voltage pulses.

structure (JCPDS PDF 01-071-4853) and $Ge_2Sb_2Te_5$ hexagonal structure (JCPDS PDF 01-073-7758), respectively. We also confirmed that the $Ge_2Sb_2Te_5$ PCM NWs were single crystalline with the same crystal orientation along the entire nanowire length, by TEM as in Figure 1(c) with inset showing TEM fast Fourier transform (FFT) diffraction patterns. Quantitative analysis by energy dispersive x-ray spectroscopy (EDX) point scanning confirms that Ge, Sb, and Te were present at an atomic ratio of 23:21:56. For electrical characterization, PCM NWs were horizontally placed on a SiO_2/Si substrates and electrical Ni/Au (30/150 nm) contacts were fabricated 3 μm apart by using an e-beam lithography lift-off process as seen in the inset of Figure 1(d). In order to improve contact properties, we etched any native amorphous oxide layer with 10% HF before the deposition of metal contact.

The completed devices were passivated with 40-nm thick SiO_2 to prevent oxidation and evaporation of PCM NWs during high current operation. Electrical transport measurements including switching characteristics were performed using an Agilent 4156C semiconductor parameter analyzer and separate pulse generator (Agilent 33250A). The DC current-voltage (*I-V*) measurement of the as-grown nanowires showed linear *I-V* characteristics with low resistance depending on nanowire diameter from 0.8 kΩ to 8 kΩ for GeTe and from 7 kΩ to 33 kΩ for $Ge_2Sb_2Te_5$, respectively. Figure 1(d) shows a representative *I-V* curve and switching characteristics by DC voltage sweep in the 28 nm diameter $Ge_2Sb_2Te_5$ NW device. The current showed an abrupt increase at a threshold voltage of ~0.93 V, which indicates that the resistance suddenly decreased by a factor of $\sim 10^2$, signaling the occurrence of an amorphous-to-crystalline phase transition. After phase transition, the current linearly increases with increasing voltage. Figure 1(e) shows a programming cycle of a 75 nm $Ge_2Sb_2Te_5$ NW memory device switched between high- and low-resistance states repeatedly. The voltage pulses for cycling are 3 V, 100 ns pulse width for RESET (amorphization or transition into high resistance) state and 1.5 V, 500 ns for SET (recrystallization or transition into low resistance) state. The fluctuations in resistance for both the amorphous and crystalline device resistances during switching cycles may be attributed to defects induced from the phase-change processes.[11,12]

As mentioned earlier, reduction of I_{reset} is desirable in PCRAM because it can facilitate scaling and reduce power consumption. We measured several diameters of both GeTe and $Ge_2Sb_2Te_5$ NWs as shown in Figures 2(a) and 2(b). In agreement with the previous reports, the writing current was decreased with NW diameter scaling from 250 nm to 90 nm for GeTe and from 100 nm to 28 nm for $Ge_2Sb_2Te_5$.[6,7] An I_{reset} pulse height down to 0.875 mA was achieved for the 91 nm GeTe NW, a significant decrease from the 5.31 mA required for the 250 nm GeTe NW. Additionally, the $Ge_2Sb_2Te_5$ NW device showed writing currents as low as 0.14 mA for the 28 nm $Ge_2Sb_2Te_5$ NW.

In order to understand the reduction of I_{reset} with decreasing NW diameter, we consider the mechanism of phase transition during the electrical pulse. It has been known that amorphization can be achieved from rapid quenching after melting by Joule heating, which can be induced by short and high current pulses. In contrast, crystallization is induced by long and low current pulses.[2] However, more recent evidence suggests that the PCM does not amorphize via melting followed by rapid quenching but via a direct solid-state process triggered by lattice distortion such as dislocations and vacancies.[13,14] Several *in-situ* TEM studies based on PCM NWs or lateral PCM structures in order to observe phase transition in phase change materials suggest this solid-state process.[11,12,14,15] Nam *et al.* reported the effect of electrical pulse on crystalline-to-amorphous

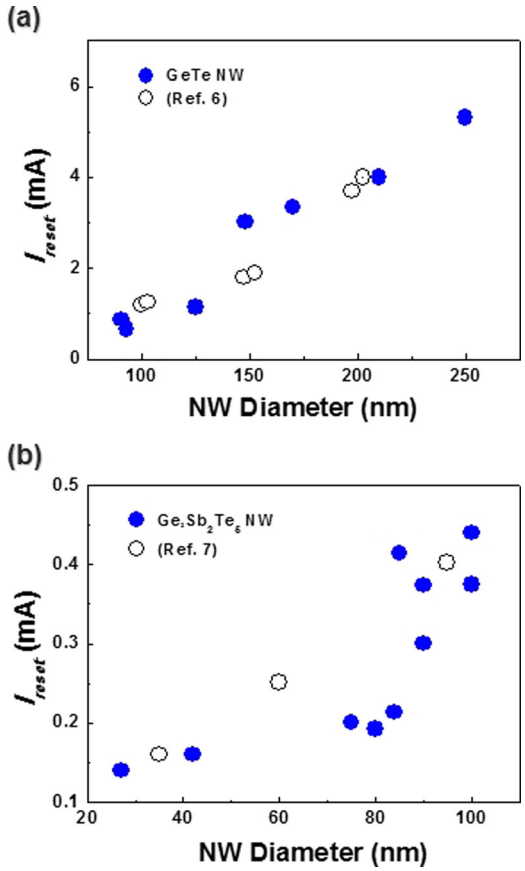

FIG. 2. Reset current (I_{reset}) dependence on NW diameter for (a) GeTe NW (90 nm–250 nm) and (b) $Ge_2Sb_2Te_5$ NW (25 nm–100 nm). Reprinted with permission from Appl. Phys. Lett. **89**(22), 223116 (2006). Copyright 2006 AIP Publishing LLC and reprinted with permission from Lee *et al.*, Nat. Nanotechnol. **2**(10), 626–630 (2007). Copyright 2007 Nature Publishing Group.

phase change in a $Ge_2Sb_2Te_5$ NWs.[14] Their *in-situ* TEM observation clearly indicates that the heat shock induced by voltage pulses can cause the formation of dislocation loops[16] in phase change materials which is followed by glide and jamming of these dislocations, triggering an amorphization. In addition, they suggest the contact between metal and nanowire could serve as the lattice vacancy source due to material incompatibility and large potential drop. They also infer the possibility of transient melting in the dislocated region due to its large resistance which induces locally concentrated Joule heating.

In order to investigate the role of contact properties between metal and PCM NWs, we first defined the size normalized I_{reset} which should be independent with nanowire diameter. When phase transition occurs via liquid-quenched or defect-induced processes, the energy consumed by the RESET operation is used for increasing the temperature of the PCM, melting for the transient liquid-state process, or inducing dislocations for the solid-state process. The heat which is used for increasing the temperature of the PCM is defined as

$$Q = c \bullet m \bullet \Delta T = c \times (d \bullet V) \times \Delta T, \tag{1}$$

where c is the specific heat capacity, m is the mass, ΔT is the temperature difference, d is the density, and V is the volume. The temperature difference is the difference between its initial temperature and either the melting temperature or the temperature which can induce dislocations depending on which process is occurring. It is noted that we ruled out the possibility of nanowire size dependent changes in melting temperature (T_m) and the temperature which can induce dislocations. Although melting behavior of nanowires have exhibited dramatically different characteristics from that of their bulk counterparts,[17,18] a decrease of T_m between nano-sized materials was not prominent until below ~15 nm.[19,20] Additionally, the previous studies have also shown that the glass transition temperature of amorphous PCM NWs with diameter ranging from 30 to 120 nm do not exhibit changes with size.[21] Finally, for the case of phase transition via a solid-state pathway, the vacancy formation energy which is used for the formation of dislocation does not significantly change in nanocrystals with size over 5 nm.[22]

Phase transition occurs when a certain volume of PCM undergoes an increase in temperature past T_m. As indicated in Figure 3(a), this volume of PCM, V, was defined as

$$V = \pi r^2 \times l, \tag{2}$$

where r is radius of NW and l is the axial length of melt-quenched volume or the region associated with inducing dislocations. Since the total input power was used for increasing the temperature of PCM during amorphization, we can compare the heat used for increasing temperature and electrical power consumption as follows:

$$\begin{aligned} P \bullet t_{reset} &= I_{reset}^2 \bullet R_{device} \bullet t_{reset} = Q \\ &= c \times (d \bullet (\pi r^2 \times l)) \times \Delta T, \end{aligned} \tag{3}$$

where t_{reset} is reset time. From Eq. (3), we observe that nanowire diameter has a linear relation with I_{reset}. When l and R_{device} are not a function of NW diameter, size normalized I_{reset} can be defined by dividing the reset current by radius of NW size $I_{normalized} = I_{reset}/r$.

Figures 4(a) and 4(b) show the resistance of NW devices (R_{device}) as a function of NW diameter for GeTe and

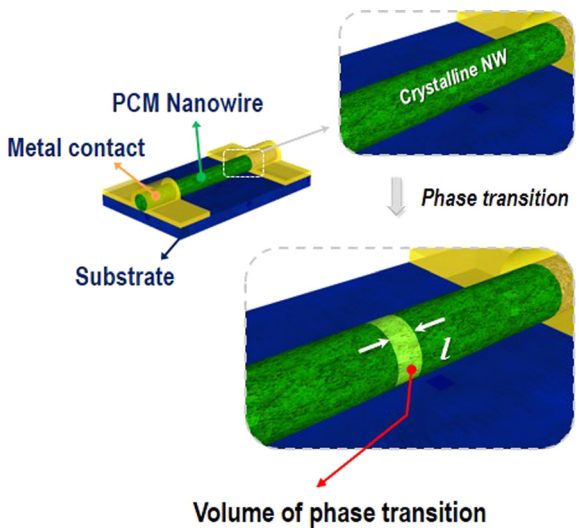

FIG. 3. Schematic of assumed conditions for phase change volume in PCM nanowires. The volume is calculated by relating switching power with nanowire dimensions. We use this method to calculate size normalized switching current size $I_{normalized} = I_{reset}/r$.

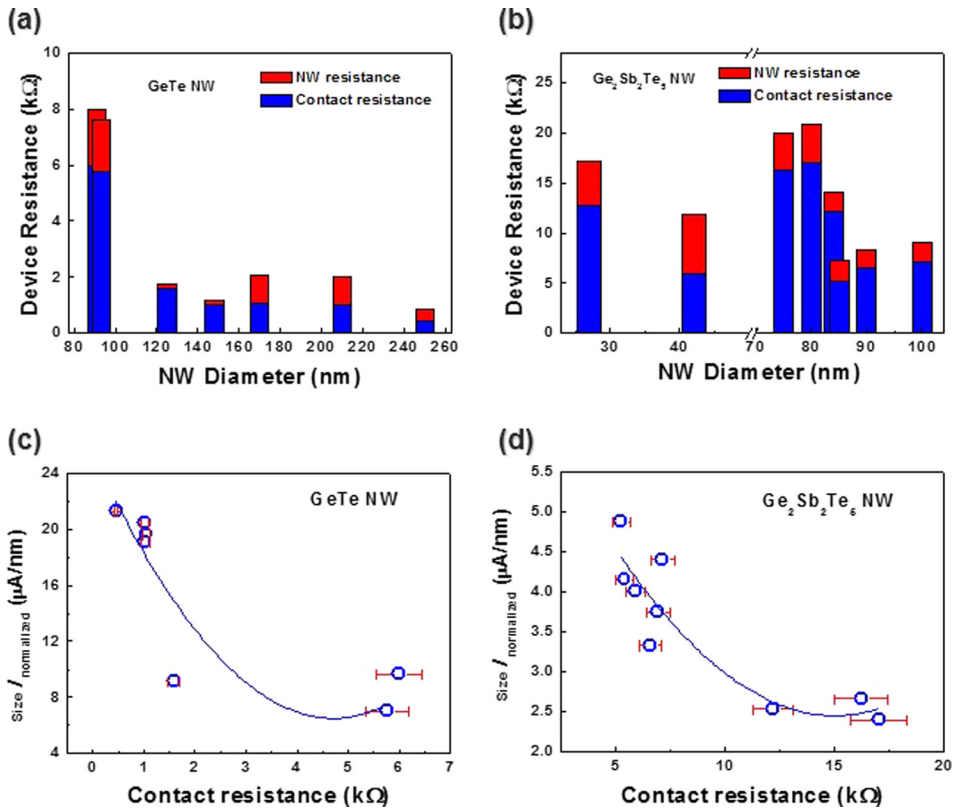

FIG. 4. Device resistance and contact resistance values calculated for (a) GeTe and (b) $Ge_2Sb_2Te_5$ for different nanowire diameters. Size normalized reset current (size $I_{normalized}$) values vs contact resistance for (c) GeTe and (d) $Ge_2Sb_2Te_5$ with data fitted by blue line.

$Ge_2Sb_2Te_5$, respectively. The proportion of contact resistance and intrinsic NW resistance to total resistance is shown in contrasting colors. We calculated the contact resistances by subtracting the intrinsic nanowire resistance measured by four-probe resistance measurement.[23] Two outer terminals were used as a current source and ground, while measuring the voltage drop across the two inner terminals. The contactless intrinsic NW resistance could then be calculated by Ohm's law as $R_{total} = V_{measured}/I_{forced}$ and then the resistivity could be calculated by the known dimensions. Contact resistance (blue) was then calculated by subtracting the contactless total NW resistance from the two-terminal measured NW resistance (red). All resistance measurements were done with the material kept in the low resistance crystalline state.

We evaluated the NW resistances by comparing the resistance difference between the total resistance and the contact resistance with the intrinsic NW resistance, which was calculated from nanowire geometry and the resistivity of crystalline PCM, $R = l/S \cdot \rho$, where l, S, and ρ are total nanowire length, cross-section area, and resistivity of NW, respectively. These measured values were consistent with the calculated NW resistance within 15% error range.

As shown in Figures 4(a) and 4(b), we found that the effect of the contact resistance on total resistance was large compared to that of the intrinsic NW resistance. We plotted the size normalized I_{reset} values as extracted above against the contact resistance for GeTe and $Ge_2Sb_2Te_5$ in Figures 4(c) and 4(d), respectively. An inversely proportional relationship between size normalized I_{reset} and contact resistance was shown for both materials shown by the fitted blue line.

Although relatively low values of contact resistance were obtained compared to the previous reports,[11] the majority of the resistance still comes from the contacts. So we can assume that the total resistance of NW device is not simply a function of NW diameter. We also assumed the axial length of active volume to be the same for all nanowires for simplicity of calculation. This assumption should be reasonable since the heat generated from the hot spot where the heating is concentrated flows along nanowire, the same material regardless of nanowire diameter. The heat dissipation from the nanowire surface was also neglected due to the thermally insulating SiO_2 shell.

We observed that the size normalized I_{reset} decreases as the contact resistance increased. This directly shows a contact resistance dependence of I_{reset}, since we have already ruled out any effect of nanowire diameter by normalization. In conventional PCRAM, the contact region serves as a heater[2] such that the material at the interface between nanowire and metal electrode would undergo phase transition. However, we found that for our devices the high resistance amorphous region is positioned in the middle of NWs by *ex-situ* SEM observation after device programming. Assuming uniform generation of heating within the nanowire, 3D thermal transport occurring near the contacts inhibit the elevation of temperature above T_m of GST. Meanwhile 1D thermal transport near the center of the NWs prevent heat loss. More importantly heat generation actually occurs at points near the center of NWs. Meister *et al.* infer that this may be attributed to the defects in the nanowire channel from simulation results.[11] Recent studies have also reported that phase change in PCM can appear anywhere along the channel not just beside the contacts[14,21] in spite of high contact resistance up to 50 times that of the NW resistance.[11]

The reduction of size normalized I_{reset} with increasing contact resistance indicates that the interfaces with high contact resistance facilitates the reset operation through

alternative non-thermal origins. Thus, we believe that high contact resistance act as a more favorable defect generation center for dislocations which can induce solid-state phase-transitions. Our result based on observation of the reduction of size normalized I_{reset} with increasing contact resistance suggests that the contacts previously used as heater in thin-film based PCRAM[2] can additionally be engineered as a defect generating site to assisting RESET operation for low power consumption by artificially increasing the contact resistance.

In summary, we investigate the scaling behavior in NW-based PCRAM resistance switching and the role of contact resistance on reduction of the I_{reset}. In order to observe the role of contact resistance on PCRAM performance, we introduced the concept of size normalized I_{reset} which is the reset current parameter independent of NW diameter. It was found that higher contact resistance reduced the normalized I_{reset} of NW PCRAM device. We suggest that the high contact resistance facilitates generation of defects from the nanowire/metal interface which then move along the nanowire channel towards the amorphization site. Our study shows opportunities for designing interfaces between PCM NW and metal contact to improve device performance.

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